Report on Guest Lecture on

"THE PRINCIPLES AND CURRENT PRACTICES & TRENDS IN ADVANCED MICRO-OPTOELECTRONIC & NANO ELECTRONIC MATERIALS MANUFACTURING / VLSI/PROCESSING, DEVICE FABRICATION & PACKAGING TECHNOLOGIES"

On 24th August,2016

Venue: Seminar Hall ,III Floor,NNRG.
Date: 24th August, 2016
Resource Person : **Dr. Veloor Narasareddy Mani, Scientist-E**
(Principal Investigator, DRDO/DST/BRNS Projects on High Pure Gallium/ Ge/ GaN & Development & Automation of Controlled Melting & Freezing & Refining Systems)
Head, High Pure Electronic Materials & Devices Division
Centre for Materials for Electronics Technology(C-MET)
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NNRG ECE department had organized a guest lecture on "The principles and current practices & trends in advanced micro-optoelectronic & nano electronic materials manufacturing / VLSI/processing, device fabrication & packaging technologies". He had also worked as Doctoral Student in Anna Technical University, Chennai / Postdoctoral Fellow/ Visiting Scientist in NTU, Chang Hua Taiwan, LCM France, CNR-Parma Italy in the areas of Semiconductor Crystals, Wafers, Thin film Structures/ Device Fabrication & VLSI / Clean Room , Packaging. Also to state that, He had delivered more than 160+ Guest/ Invited/ Keynote lectures/ addresses over years to EEE/ECE/EIE/ Nanotechnology/VLSI (B.E & M.Tech) students in various Universities/ NITs/ Engineering Colleges (IEEE-Students Chapters/MRSI/SSI/IPS / Techno-Fests. etc. Forums/ Meetings/ Faculty Development Programs/ Orientation/Motivation Programs/Workshops/ Schools/ DST Inspire Science Camps/ Conferences) in Telengana, AP, Tamilnadu, Karnataka, Orissa etc.

In this overview talk,He covered topics like development of ultra high and nano pure (7N) gallium, indium and their crystals, wafers and the recent nano-scaled systems, which are required for epitaxial opto and nano- electronics and optoelectronics will be highlighted. The talk also cover technological issues namely multi-pass zone-refining, directional solidification and associated chemical engineering, instrument development aspects, preparation of bulk crystals and substrates including VLSI principles and practices. The bird's eye view will be on the principles and practices pertaining to the crystal and substrate preparation (purity test, in-situ synthesis of GaAs compound, GaAs crystal preparation, crystal sawing, lapping, edge profiling, wafer surface etching, inspection & marking, wafer polishing, post polish cleaning, flatness testing and epitaxy and device fabrication concepts (epitaxy, creation of active regions, photo resist / oxide formation, patterning, chip etching, doping, chip section development, source, drain, gate formation (regions), connecting the regions and outer pins, building up patterned layers and final circuit design aspects. The class clean and green processing scheme(s) for sample homogenization, preparation, processing analysis and packaging, the usage of the class clean room (1000), clean benches (100) environment and characterization issues will be dealt with.

A total of 220 students have attendant the lecture which covered II B.Tech syllabus EDC, III B.Tech syllabus IC Technology and IV B.tech syllabus VLSI Design.

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